U.S. Department of Commerce, Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

Application No.:	09/849,005
Filing Date:	May 4, 2001
First Named Inventor:	Chian-Min Richard Ho
Group Art Unit:	2123
Examiner Name:	Frejd, Russell Warren
Confirmation No.:	1848
Attorney Docket No.:	0IN006-1C US

U.S. Patent Documents

*Examiner Intials		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
RF	1	5,729,554	03/17/98	Weir et al.	714	31	
RF	2	5,623,499	03/22/97	Ko et al.	395	500.06	
RF	3	5,600,787	02/04/97	Underwood et al.	714	30	
RF	4	5,654,657	08/05/97	Pearce	327	163	
RF	5	5,680,332	10/21/97	Riami et al.	703	13	
RF	6	5,479,414	12/026/95	Keller et al.	714	726	
RF	7	5,202,889	03/13/93	Aharon et al.	714	739	

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

RF	8	Singer, S. ; Vanetsky, L.; "Next Generation (NGTG) for Digital Circuits", Proceedings of IEEE AUTOTESTCON, pp. 105 -112, 1997 ✓
RF	9	Liang et al., "Identifying Invalid States for Sequential Circuit Test Generation", IEEE Trans. On Computer-Aided Design of Int. Circuits and Systems, Vol. 16, Issue 9, pp. 1025-1033, September 1997. ✓
RF	10	Liang et al., "Identifying Invalid States for Sequential Circuit Test Generation", Proc. Of the Fifth Asian Test Symposium 1996, pp. 10-15, November 1996 ✓
RF	11	Camurati et al., "Efficient Verification of Sequential Circuits on a Parallel System", Proc. Third European Conference on Design Automation, pp. 64-68, March 1992. ✓

Examiner: RUSSELL FREJD	Date Considered: 26 JAN 04

* Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication with applicant.

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RF	12	5,539,652	07/23/96	Tegethoff	364	490	
RF	13	5,638,381	06/10/97	Cho et al.	371	22.4	
RF	14	5,862,149	01/19/99	Carpenter et al.	371	22.3	
RF	15	6,292,765	09/18/01	Ho et al.	703	14	
RF	16	6,175,946	01/16/01	Ly et al.	716	4	
RF	17	6,609,229	08/19/003	Ly et al.	716	4	
RF	18	5,661,661	08/26/97	Gregory et al.	364	489	

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

RF	19	Kant et al., "Synthesizing Robust Data Structures – An Introduction", IEEE Trans. On Computers, pp. 161-173, 1990.
RF	20	Caporossi et al., "Rule Checking at the Register Level", IEEE Spectrum, pp. 72-73, 1996.
RF	21	Vinnakota et al., "Design of Multiprocessor Systems for Concurrent Error Detection and Fault Diagnosis", IEEE, pp. 504-511, 1991.
RF	22	Benso, et al., "Exploiting HDLs for Circuits Fault Tolerance Assessments", IEEE, pp. 212-216, 1997.
RF	23	Amato et al., "Checking Linked Data Structures", IEEE, pp. 164-173, 1994.

Examiner:	Date Considered:
Russell Frejd	26 JAN 04

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Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

RF	24	Devadas et al., "An Observability-Based Code Coverage Metric for Functional Simulation", IEEE 1996, pp. 418-425.
RF	25	Vincentelli et al., "Verification of Electronic Systems", 33rd Design Automation Conference, Las Vegas, Proceedings 1996, pp. 106-111.
RF	26	K.L. McMillan, "Fitting Formal Methods into the Design Cycle", 31st ACM/IEEE 1994, pp. 314-319.
RF	27	Ho et al., "Architecture Validation for Processors", Proceedings 22nd Annual Internationals, Symposium on Computer Architecture, June 22-24, 1995, IEEE Computer Society, pp.404-413.
RF	28	Ho et al., "Validation Coverage Analysis for Complex Digital Designs", IEEE/ACM International Conference On Computer-Aided Design, November 10-14 1996, pp.146-151
RF	29	Jones et al., "The Automatic Generation of Functional Test Vectors for Rambus Designs", 33rd Design Automation Conference IEEE Circuits & Systems Society, 1996
RF	30	Geist et al., " Coverage-Directed Test Generation Using Symbolic Techniques", pp. 142-158, First Int'l Conference FMCAD '96 Palo Alto, CA USA, November 6-8, 1996 Proceedings.
RF	31	Chian-Min Richard Ho, "Validation Tools For Complex Digital Designs", PhD Dissertation, Stanford University, November 1996, pages 6-15.

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